

Notice of References Cited	Application/Control No. 09/853,968	Applicant(s)/Patent Under Reexamination MARU, TSUGUO	
	Examiner Jacob Meek	Art Unit 2637	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,933,462	08-1999	Viterbi et al.	375/341
	B	US-6,161,209	12-2000	Moher, Michael I.	714/780
	C	US-6,343,368	01-2002	Lerzer, Jurgen	714/796
	D	US-6,484,283	11-2002	Stephen et al.	714/786
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Pipelined architectures for the Viterbi algorithm; Boo, M.; Brugera, J.D.; TENCON '97. IEEE Region 10 Annual Conference. Speech and Image Technologies for Computing and Telecommunications', Proceedings of IEEE Volume 1, 2-4 Dec. 1997 Page(s):239 - 242 vol
	V	A Viterbi decoder architecture based on parallel processing elements; Meier, S.R.; Global Telecommunications Conference, 1990, and Exhibition. 'Communications: Connecting the Future', GLOBECOM '90., IEEE; 2-5 Dec. 1990 Page(s):1323 - 1327 vol.2
	W	A 1-Gb/s, four-state, sliding block Viterbi decoder; Black, P.J.; Meng, T.H.-Y.; Solid-State Circuits, IEEE Journal of Volume 32, Issue 6, June 1997 Page(s):797 - 805
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.